POWER CONTROL CIRCUIT FOR OPTICAL INFORMATION RECORDING DEVICE

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BACKGROUND OF THE INVENTION

Field of the Invention:

[0001] This invention relates in general to a power control circuit for an optical information recording device. More specifically, this invention relates to a power control circuit suitable for a high-speed optical information recording device.

Description of Related Art:

[0002] The optical information recording apparatus, such as a recordable (or re-writable) optical disk drive, becomes wide-used and popular because of a high demand of high capacity back-up. When a recordable optical disk drive records data or information to a Recordable/Re-Writable Compact Disc (CD-R/CD-RW), beam for recording data is generated by a laser diode. The laser diode has to provide three optical signals with different power during the entire recording process. The data region of an optical disc will alter its state in response to the optical signal with specified power.

[0003] Fig. 1 schematically shows a graph that power of an optical signal

during writing varied with respect to its corresponding data area of an optical disc. The data area of a re-writable optical disc includes a space region and a mark region. The mark region records data that is encoded by logic "1" and logic "0". The laser diode has to generate an optical signal with erase power P_{ERASE} to illuminate the optical disc when the laser beam reaches the space region. In addition, the laser diode has to generate optical signals with write power P_{WRITE} and bias power P_{BIAS} alternately to illuminate the optical disc when the laser beam reaches the mark region. When data is written to the mark region, the required times for generating the write power P_{WRITE} and the bias power P_{BIAS} is determined by the characteristic of the optical disc and the specification of data to be recorded.

[0004] However, the characteristic of the laser diode varies with the environment temperature and time. During the recording process, as the recording time increases, the temperature of the laser diode increases. Namely, under the condition that the driving signals inputted to the laser diode are the same, the laser diode outputs optical signals having different power due to different temperature. When the laser diode is aged, the optoelectronic characteristic of the laser diode maybe change. Therefore, a power control circuit for compensating power variation due to change of the optical characteristic of the laser diode is highly required. If the bias power is not compensated, the laser diode may completely turn off during certain period, and to turn on the laser diode again requires a larger current or a longer time.

[0005] Fig. 2 shows a conventional power control circuit for a recordable

optical disc. The laser diode D1 receives the driving signal from the laser diode driving circuit 202 to generate a corresponding optical signal. The optical signal is illuminated to an optical disc (not shown) for recording data on the optical disc. In order to compensate the optical signal, a photodiode D2 is used for sensing the optical signal emitted from the laser diode D1 to generate a corresponding power sampling signal PI. The power sampling signal PI comprises an erase period corresponding to an optical signal with erase power of P_{ERASE}, a write period corresponding to an optical signal with write power of P_{WRITE}, a bias period corresponding to an optical signal with bias power of P_{BIAS}. The power sampling signal PI is transmitted to an erase-period sample-and-hold circuit 204, a write-period sample-and-hold circuit 206, and a bias-period sample-and-hold circuit 208, respectively.

[0006] The erase-period sample-and-hold circuit 204 is controlled by an erase sampling control signal ESC to sample the power sampling signal PI within the erase period, by which an erase-period sample-and-hold signal EPSH is generated and then fed-back to a feedback control circuit 205. The feedback control circuit 205 converts the erase-period sample-and-hold signal EPSH to a signal that is acceptable to the laser diode driving circuit 202 and then transmits the converted signal to the laser diode driving circuit 202. The write-period sample-and-hold circuit 206 is controlled by a write sampling control signal WSC to sample the power sampling signal PI within the write period, by which a write-period sample-and-hold signal WPSH is generated and then fed-back to a feedback control circuit 205. The feedback control circuit 205 converts the write-period sample-and-hold signal WPSH to a signal that is acceptable to the

laser diode driving circuit 202 and then transmits the converted signal to the laser diode driving circuit 202. The bias-period sample-and-hold circuit 208 is controlled by a bias sampling control signal BSC to sample the power sampling signal PI within the bias period, by which a bias-period sample-and-hold signal BPSH is generated and then fed-back to the feedback control circuit 205. The feedback control circuit 205 converts the bias-period sample-and-hold signal EPSH to a signal that is acceptable to the laser diode driving circuit 202 and then transmits the converted signal to the laser diode driving circuit 202. Accordingly, the laser diode driving circuit 202 alters the driving signal that is outputted to the laser diode D1 according to the erase-period sample-and-hold signal EPSH, the write-period sample-and-hold signal WPSH, and the bias-period sample-and-hold signal BPSH so as to adjust the erase power, the write power and the bias power of the optical signal, by which the compensation for the optical signal is completed.

[0007] Fig. 3 shows waveforms of the power sampling signal PI, the write sampling control signal WSC and the bias sampling control signal BSC in Fig. 2. Fig. 3 only shows the waveforms in the write period and the bias period of the power sampling signal PI. Operation for a general sample-and-hold circuit includes a sampling operation and a holding operation. Therefore, when the write sampling control signal WSC is at high level, the write period sample-and-hold circuit 206 samples the power sampling signal PI, and when the write sampling control signal WSC is at low level, the write period sample-and-hold circuit 206 holds the level of the power sampling signal PI that is sampled as the write sampling control signal WSC is transient from high level

to low level. The bias period sample-and-hold circuit 208 is controlled by the bias sampling control signal BSC in the same manner. Accordingly, the write period sample-and-hold circuit 206 is controlled by the write sampling control signal WSC to sample the power sampling signal PI when the write sampling control signal WSC becomes high level within the write period of the power sampling signal PI, by which the signal level of the power sampling signal PI is obtained. This sampled signal level corresponds to the write power of the light beam emitted by the laser diode within the write period. Similarly, the bias period sample-and-hold circuit 208 is controlled by the bias sampling control signal BSC to sample the power sampling signal PI when the bias sampling control signal BSC becomes high level within the bias period of the power sampling signal PI, by which the signal level of the power sampling signal PI is obtained. This sampled signal level corresponds to the bias power of the light beam emitted by the laser diode within the bias period.

[0008] The sampling time for the general sample-and-hold circuit has to be larger than a specified value so that the sample-and-hold circuit can operate normally. As the technology of the recordable optical disk drive is highly developed, a high-speed recordable optical disk drive becomes the main product gradually in the market. However, if the recordable optical disk drive is operated in high speed, the frequency of power sampling signal PI increases, causing that intervals of the write period and the bias period are shortened. In the situation, because the general sample-and-hold circuit is not fast enough, the sampling time becomes too long so that the signal levels in the write period and the bias period of the sampling signal PI cannot be correctly sampled.

[0009] Fig. 4 shows relevant high frequency waveforms of the power sampling signal PI, the write sampling control signal WSC and the bias sampling control signal. When the frequency of the power sampling signal PI increases and the write period and the bias period are shortened, the conventional power control circuit of the recordable optical disk drive cannot sample the signal levels correctly because of the speed limitation of the write sample-and-hold circuit 206 and the bias sample-and-hold circuit 208, thereby the optical signals from the laser diode cannot be correctly compensated. However, if a high-speed sample-and-hold circuit is used, cost becomes higher. Therefore, it is necessary to develop a power control circuit that is suitable for a high-speed recordable optical disk drive without the need of high cost sample-and-hold circuit.

SUMMARY OF THE INVENTION

[0010] According to the foregoing description, an object of this invention is to provide a power control circuit for an optical information recording apparatus. Due to its low cost, the power control circuit of the invention is suitable for a high-speed optical information recording apparatus.

[0011] According to the object(s) mentioned above, a power control circuit is provided. The power control circuit is used for an optical disk drive, wherein the optical disk drive has a diode driving circuit, a light emitting diode and a photo diode. The diode driving circuit is used for outputting a driving signal to the light emitting diode, the light emitting diode generates an optical signal

corresponding to the driving signal, and the photo diode is used for sensing the optical signal to generate a power sampling signal correspondingly. The power control circuit comprises an erase-period sample-and-hold circuit, a peak envelope acquiring circuit, a bottom envelope acquiring circuit, a write-period sample-and-hold circuit and a bias-period sample-and-hold circuit. The erase-period sample-and-hold circuit is used for receiving the power sampling signal, and then outputting an erase-period sample-and-hold signal to the diode driving circuit. The peak envelope acquiring circuit is used for receiving the power sampling signal and outputting a peak envelope signal. The bottom envelope acquiring circuit is used for receiving the power sampling signal and outputting a bottom envelope signal. The write-period sample-and-hold circuit is used for receiving the peak envelope signal, and outputting a write-period sample-and-hold signal to the diode driving circuit. The bias-period sample-and-hold circuit is used for receiving the bottom envelope signal, and outputting a bias-period sample-and-hold signal to the diode driving circuit. Thereby, the diode driving circuit alters the driving signal according to the erase-period sample-and-hold signal, the write-period sample-and-hold signal, and the bias-period sample-and-hold signal so that power of the optical signal is adjusted.

[0012] The invention further provides a power control circuit for an optical disk drive, wherein the optical disk drive has a diode driving circuit, a light emitting diode and a photo diode. The diode driving circuit is used for outputting a driving signal to the light emitting diode, the light emitting diode generates an optical signal corresponding to the driving signal, and the photo diode is used

for sensing the optical signal to generate a power sampling signal correspondingly. The power control circuit comprises an erase-period sample-and-hold circuit, a peak envelope sample-and-hold circuit and a bottom envelope sample-and-hold circuit. The erase-period sample-and-hold circuit is used for receiving the power sampling signal, and then outputting an erase-period sample-and-hold signal to the diode driving circuit. The peak envelope sample-and-hold circuit is used for receiving the power sampling signal and outputting a write-period sample-and-hold signal to the diode driving circuit. The bottom envelope sample-and-hold circuit is used for receiving the power sampling signal and outputting a bias-period sample-and-hold signal to the diode driving circuit. Thereby, the diode driving circuit alters the driving signal according to the erase-period sample-and-hold signal, the write-period sample-and-hold signal, and the bias-period sample-and-hold signal so that power of the optical signal is adjusted.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] While the specification concludes with claims particularly pointing out and distinctly claiming the subject matter which is regarded as the invention, the objects and features of the invention and further objects, features and advantages thereof will be better understood from the following description taken in connection with the accompanying drawings in which:

[0014] Fig. 1 schematically shows a graph that power of an optical signal during writing varies with respect to its corresponding a data area of an optical

disc;

[0015] Fig. 2 shows a conventional power control circuit for a recordable optical disk drive;

[0016] Fig. 3 shows waveforms of the power sampling signal PI, the write sampling control signal WSC and the bias sampling control signal BSC in Fig. 2;

[0017] Fig. 4 shows relevant high frequency waveforms of the power sampling signal PI, the write sampling control signal WSC and the bias sampling control signal;

[0018] Fig. 5 schematically shows a block diagram of a power control circuit for an recordable optical disk drive according to the first embodiment of the invention;

[0019] Fig. 6 shows waveforms of the power sampling signal PI, the peak envelope signal PE and the bottom envelope signal BE in Fig. 5;

[0020] Fig. 7 shows an exemplary block diagram of the peak envelope acquiring circuit in Fig. 5;

[0021] Fig. 8 schematically shows an example of relevant waveforms of the power sampling signal PI, the first output signal A, the second output signal B, the third output signal C and the fourth output signal in the peak envelope acquiring circuit shown in Fig. 7;

[0022] Fig. 9 schematically shows a block diagram of a power control circuit for an recordable optical disk drive according to the second embodiment of the invention;

[0023] Fig. 10A shows an exemplary block diagram of the peak envelope sampling/holding circuit in Fig. 9;

[0024] Fig. 10B shows an exemplary block diagram of the bottom envelope sampling/holding circuit in Fig. 9; and

[0025] Fig. 11 schematically shows relevant waveforms of the power sampling signal PI, the write sampling control signal WSC, the output signal S, the output signal Q, the write-period sample-and-hold signal WPSH, the bias sampling control signal BSC, the output signal S', the output signal Q', and the bias-period sample-and-hold signal BPSH in the peak and bottom envelope sampling/holding circuits shown in Figs. 10A and 10B.

DESCRIPTION OF THE PREFERRED EMBODIMENT

[0026] A power sampling signal from a photodiode is transmitted to a peal envelope acquiring circuit and a bottom envelope acquiring circuit and then sampled and held, which is fed-back to a laser diode driving circuit. The laser diode driving circuit alters a driving signal emitted to the laser diode according to the fed-back signal to adjust the power of the optical signal emitted from the laser diode. Therefore, a low-cost and high-speed recordable optical disk drive can be made.

<<First Embodiment>>

[0027] Fig. 5 schematically shows a block diagram of a power control circuit for a recordable optical disk drive according to the first embodiment of the invention. The laser diode D1 is used for receiving a driving signal from a laser diode driving circuit 502 to generate a corresponding optical signal. The optical signal is illuminated to an optical disc (not shown) for recording data on the optical disc. In order to compensate the optical signal, a photodiode D2 is used for sensing the optical signal emitted from the laser diode D1 to generate a corresponding power sampling signal PI. The power sampling signal PI is transmitted to an erase-period sample-and-hold circuit 504, a write-period sample-and-hold circuit 506, a peak envelope acquiring circuit 510 and a bottom envelope acquiring circuit 512, respectively.

[0028] The peak envelope acquiring circuit 510 is used for detecting an envelope formed by a positive peak of the power sampling signal PI so that a peak envelope signal PE is generated and outputted. The bottom envelope acquiring circuit 512 is used for detecting an envelope formed by a negative peak of the power sampling signal PI so that a bottom envelope signal BE is generated and outputted. The peak envelope signal PE and the bottom envelope signal BE are respectively transmitted to the write-period sample-and-hold circuit 506 and the bias-period sample-and-hold circuit 508.

[0029] Additionally, the erase-period sample-and-hold circuit 504 is controlled by an erase sample-and-hold control signal ESC to sample the power sampling

signal PI within the erase period, by which an erase-period sample-and-hold signal EPSH is generated and fed-back to the feedback control circuit 505. The feedback control circuit 505 converts the erase-period sample-and-hold signal EPSH to a signal that is acceptable to the laser diode driving circuit 502 and then transmits the converted signal to the laser diode driving circuit 502. The erase-period sample-and-hold circuit 506 is controlled by a write sample-and-hold control signal WSC to sample the peak envelope signal PE, by which a write-period sample-and-hold signal WPSH is generated and fed-back to the feedback control circuit 507. The feedback control circuit 507 converts the write-period sample-and-hold signal WPSH to a signal that is acceptable to the laser diode driving circuit 502 and then transmits the converted signal to the laser diode driving circuit 502. The bias-period sample-and-hold circuit 508 is controlled by a bias sample-and-hold control signal BSC to sample the bottom envelope signal BE, by which a bias-period sample-and-hold signal BPSH is generated and fed-back to the feedback control circuit 507. The feedback control circuit 507 converts the bias-period sample-and-hold signal BPSH to a signal that is acceptable to the laser diode driving circuit 502 and then transmits the converted signal to the laser diode driving circuit 502. Accordingly, the laser diode driving circuit 502 alters the driving signal that is outputted to the laser diode D1 according to the erase-period sample-and-hold signal EPSH, the write-period sample-and-hold signal WPSH, and the bias-period sample-and-hold signal BPSH so as to adjust the magnitudes of the erase power, the write power and the bias power of the optical signal, by which the compensation for the optical signal is completed.

[0030] Fig. 6 shows waveforms of the power sampling signal PI, the peak envelope signal PE and the bottom envelope signal BE in Fig. 5. The envelope formed by the positive peaks of the power sampling signal PI is depicted as a dash line 602, and the envelope formed by the negative peaks of the power sampling signal PI is depicted as a dash line 604. The peak envelope acquiring circuit 510 and the bottom envelope acquiring circuit 512 detect respectively the envelopes (as shown in dash lines 602, 604) formed by the positive peaks and the negative peaks of the power sampling signal PI, and then generate the peak envelope signal PE and the bottom envelope signal BE that correspond to dash lines 602, 604 respectively. The peak envelope signal PE can be set as an average level of the power sampling signal PI within the write period, and the bottom envelope signal BE can be set as an average level of the power sampling signal PI within the bias period. The frequencies of the peak envelope signal PE and the bottom envelope signal BE are much lower than the frequency of the power sampling signal PI.

[0031] As described above, in stead of directly sampling the power sampling signal PI having a much higher frequency, the peak envelope signal PE and the bottom envelope signal BE that have lower frequencies are respectively sampled by the write-period sample-and-hold circuit 506 and the bias-period sample-and-hold circuit 508. Accordingly, it can effectively prevent from that the frequency of the power sampling signal PI is too high to get its signal level accurately by the sample-and-hold circuit. According to the invention, due to low frequencies of the peak envelope signal PE and the bottom envelope signal BE, a general low-speed sample-and-hold circuit can be normally operated to

compensate the optical signals emitted from the laser diode D1. Unlike the conventional one, no sample-and-hold circuit that is operated under high frequency is required, and therefore cost for high-speed sample-and-hold circuit can be saved.

[0032] Fig. 7 shows an exemplary block diagram of the peak envelope acquiring circuit in Fig. 5. The peak envelope acquiring circuit 510 comprises a positive half-wave rectifier 702, a multiplexer 704, a Schmitt trigger 706, a peak detector 708 and an amplifier 710. The power sampling signal PI is inputted to the positive half-wave rectifier 702. The positive half-wave rectifier 702 then outputs a first output signal A having the positive levels of the power sampling signal PI. The first output signal A is transmitted to the multiplexer 704 and the Schmitt trigger 706 respectively. The Schmitt trigger 706 generates a second output signal B in response to the first output signal A. A third output signal C from the amplifier 710 is also inputted to the multiplexer 704. The second output signal B is transmitted to a selection terminal SEL of the multiplexer 704 for selecting the first output signal A or the third output signal C as a fourth output signal D, which is then transmitted to the peak detector 708. The peak detector 708 detects a peak value of the fourth output signal D that is inputted to the amplifier 710. The gain of the amplifier 710 is 1. The amplifier 710 possesses a holding function for filtering the high frequency signals, and outputs the third output signal C. Therefore, the third output signal C from the amplifier 710 corresponds to a low frequency signal of the peak of the fourth output signal D. The peak envelope acquiring circuit 510 outputs the third output signal C as the peak envelope signal PE.

[0033] Fig. 8 schematically shows an example of relevant waveforms of the power sampling signal PI, the first output signal A, the second output signal B, the third output signal C and the fourth output signal in the peak envelope acquiring circuit shown in Fig. 7. As shown, the first output signal A corresponds to positive levels of the power sampling signal PI . When the level of the first output signal A is higher than the level of a high triggering level TH of the Schmitt trigger circuit 706, the second output signal B is logic "1", and when the level of the first output signal A is lower than the level of a low triggering level TL of the Schmitt trigger circuit 706, the second output signal B is logic "0". When the second output signal B is logic "1", the multiplexer 704 outputs the first output signal A as the fourth output signal D, and when the second output signal B is logic "0", the multiplexer 704 outputs the third output signal C as the fourth output signal D. After the fourth output signal D is processed by the peal detector 708 and the amplifier 710, the third output signal C varies with the peak values of the fourth output signal D. Therefore, the third output signal C is the envelope formed by the positive peaks of the power sampling signal PI.

[0034] Similarly, the bottom envelope acquiring circuit 512 is similar to the peak envelope acquiring circuit 510, which a negative half-wave rectifier 702 is used for replacing the positive half-wave rectifier 702 in Fig. 7 to get the bottom envelope signal BE. Although the peak envelope acquiring circuit 510 is used for the description, but it is not to limit the scope of the invention. Any circuit capable of detecting the envelope formed by the positive peaks and the envelope formed by the negative peaks of the power sampling signal PI can

serve as the envelope acquiring circuit of the invention. In addition, the application of the invention is not only the recordable optical disk drives, but also other optical disk drive systems. Moreover, the laser diode of the invention can be replaced by any other type of light emitting diodes.

<<Second Embodiment>>

[0035] Fig. 9 schematically shows a block diagram of a power control circuit for an recordable optical disk drive according to the second embodiment of the invention. A laser diode D3 receives a driving signal outputted from a laser diode driving circuit 902 to generate a corresponding optical signal. A photodiode D4 is used for sensing the optical signal emitted from the laser diode D3 to generate a corresponding power sampling signal PI. The power sampling signal PI is transmitted to an erase-period sample-and-hold circuit 904, a peak envelope sample-and-hold circuit 904 and a bottom envelope sample-and-hold circuit 908, respectively.

[0036] The erase-period sample-and-hold circuit 904 is controlled by an erase sample-and-hold control signal ESC to sample the power sampling signal PI within the erase period, by which an erase-period sample-and-hold signal EPSH is generated and fed-back to the feedback control circuit 905. The feedback control circuit 905 converts the erase-period sample-and-hold signal EPSH to a signal that is acceptable to the laser diode driving circuit 902 and then transmits the converted signal to the laser diode driving circuit 902.

[0037] The peak envelope sample-and-hold circuit 906 is controlled by a write

sample-and-hold control signal WSC to sample the power sampling signal PI within the write period, by which a write-period sample-and-hold signal WPSH is generated and fed-back to the feedback control circuit 907. The feedback control circuit 907 converts the write-period sample-and-hold signal WPSH to a signal that is acceptable to the laser diode driving circuit 902 and then transmits the converted signal to the laser diode driving circuit 902.

[0038] The bottom envelope sample-and-hold circuit 908 is controlled by a bias sample-and-hold control signal BSC to sample the power sampling signal PI within the bias period, by which a bias-period sample-and-hold signal BPSH is generated and fed-back to the feedback control circuit 909. The feedback control circuit 909 converts the bias-period sample-and-hold signal BPSH to a signal that is acceptable to the laser diode driving circuit 902 and then transmits the converted signal to the laser diode driving circuit 902.

[0039] Accordingly, the laser diode driving circuit 902 alters the driving signal that is outputted to the laser diode D3 according to the erase-period sample-and-hold signal EPSH, the write-period sample-and-hold signal WPSH, and the bias-period sample-and-hold signal BPSH so as to adjust the erase power, the write power and the bias power of the optical signal, by which the compensation for the optical signal is completed.

[0040] Fig. 10A shows an exemplary block diagram of the peak envelope sampling/holding circuit in Fig. 9; and Fig. 10B shows an exemplary block diagram of the bottom envelope sampling/holding circuit in Fig. 9. The peak

envelope sample-and-hold circuit 906 comprises a positive half-wave rectifier 1002, a multiplexer 1004 and a peak detector 1008. The power sampling signal PI and the write-period sample-and-hold signal WPSH are inputted to the multiplexer 1004. The multiplexer 1004 receives the write sampling control signal WSC to generate an output signal S corresponding to power sampling signal PI and the write-period sample-and-hold signal WPSH. The output signal S is then transmitted to the positive half-wave rectifier 1002 to sample the positive levels of the power sampling signal PI as an output signal Q. The output signal Q is then transmitted to the peak detector 1008 to generate the write-period sample-and-hold signal WPSH.

[0041] Similarly, as shown in Fig. 10B, the bottom envelope sample-and-hold circuit 908 comprises a negative half-wave rectifier 1012, a multiplexer 1014 and a peak detector 1018. The power sampling signal PI and the bias-period sample-and-hold signal BPSH are inputted to the multiplexer 1014. The multiplexer 1014 receives the bias sampling control signal BSC to generate an output signal S' corresponding to the power sampling signal PI and the bias-period sample-and-hold signal BPSH. The output signal S is then transmitted to the negative half-wave rectifier 1012 to sample the negative levels of the power sampling signal PI as an output signal Q'. The output signal Q' is then transmitted to the peak detector 1018 to generate the bias-period sample-and-hold signal BPSH.

[0042] Fig. 11 schematically shows relevant waveforms of the power sampling signal PI, the write sampling control signal WSC, the output signal S, the output

signal Q, the write-period sample-and-hold signal WPSH, the bias sampling control signal BSC, the output signal S', the output signal Q', and the bias-period sample-and-hold signal BPSH in the peak and bottom envelope sampling/holding circuits shown in Figs. 10A and 10B. Fig. 11 shows waveform diagrams when the laser beam reaches the space region of the optical disc in time intervals T1 and T3, and waveform diagrams when the laser beam reaches the mark region of the optical disc in time interval T2. When the write sampling control signal WSC is logic "1", the multiplexer 1004 outputs the power sampling signal PI as the output signal S, and when the write sampling control signal WSC is logic "0", the multiplexer 1004 outputs the write-period sample-and-hold signal WPSH as the output signal S. The output signal Q corresponds to the output signal S with positive level. The write-period sample-and-hold signal WPSH corresponds to the peaks of the output signal Q.

[0043] When the bias sampling control signal BSC is logic "1", the multiplexer 1014 outputs the power sampling signal PI as the output signal S', and when the bias sampling control signal BSC is logic "0", the multiplexer 1014 outputs the bias-period sample-and-hold signal BPSH as the output signal S'. The output signal Q corresponds to the output signal S' with negative level. The bias-period sample-and-hold signal BPSH corresponds to the peaks of the output signal Q'.

[0044] As shown in Figs. 9 and 10A~10B, because the write sampling control signal WSC and the bias sampling control signal BSC are used for controlling the multiplexers 1004, 1014 respectively, for example logic "1" in the time

intervals T1, T3 and logic "0" in the time intervals T2, the frequencies of the write sampling control signal WSC and the bias sampling control signal BSC of the invention are much lower than the frequency of the power sampling signal PI. For a high-speed optical information recording apparatus, unlike the conventional power control circuit that requires a sample-and-hold circuit capable of being operated in high frequency, although the frequency of the power sampling signal PI is still very high, but the write sampling control signal WSC and the bias sampling control signal BSC with lower frequencies are only required to achieving its purposes. Therefore, cost of the device can be significantly saved.

[0045] According to the power control circuit for the optical information recording apparatus of the invention, a low-speed sample-and-hold at low cost can be used for acquiring the signal level of the high-frequency power sampling signal, so that the optical signal can be properly adjusted for an application of a high-speed optical recording disc. This invention is particularly suitable for low-cost and high-speed optical information recording apparatus.

[0046] While the present invention has been described with a preferred embodiment, this description is not intended to limit our invention. Various modifications of the embodiment will be apparent to those skilled in the art. It is therefore contemplated that the appended claims will cover any such modifications or embodiments as fall within the true scope of the invention.